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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,644	07/23/2003	Kyuichi Takimoto	030879	6904

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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,644	TAKIMOTO ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 7, 14, 15 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Bazinet et al (US 5,627,460).

Claims 1, 2 and 7; Bazinet et al, figures 1-3, disclose a control circuit (30) for controlling an output voltage of a DC/DC converter (10), the DC/DC converter includes a main switching element and a synchronous switching element (12, 14), the control circuit comprising: a pulse signal generation circuit (32) which generates a pulse (62) signal for controlling the DC/DC converter based on the output voltage (Vout); and a drive signal generation circuit (34) connected to the pulse signal generation circuit (32) , the drive signal generation circuit generates first and second drive signals (38, 40) using the pulse signal for respective supply to the main switching element and the synchronous switching element such that the main switching element and the synchronous switching element are turned ON and OFF alternately at different timings,

and the drive signal generation circuit generates the first drive signal such that the first drive signal has substantially the same pulse width as that of the pulse signal (see figure 3: 114, 116); furthermore, the drive signal generation circuit (34) generates the second drive signal such that the second drive signal has a larger pulse width than the first drive signal using the pulse signal and the first drive signal (see figure 3: 118).

Claims 14 and 15; Bazinet et al, figures 1-3, disclose a DC/DC converter comprising: a main switching element and a synchronous switching element (12, 14); a smoothing circuit (18, 20) connected to a node between the main switching element and the synchronous switching element, the smoothing circuit generating an output voltage; and a control circuit (30) which controls the output voltage by supplying a first drive signal to the main switching element and supplying a second drive signal to the synchronous switching element (38, 40), the control circuit including: a pulse signal generation circuit (34) which generates a pulse signal for controlling the output voltage based on the output voltage (Vout); and a drive signal generation circuit (34) connected to the pulse signal generation circuit, the drive signal generation circuit generating the first and second drive signals by using the pulse signal such that the main switching element and the synchronous switching element are turned ON and OFF alternately at different timings, and the drive signal generation circuit (34) generating the first drive signal such that the first drive signal has substantially the same pulse width as that of the pulse signal (see figure 3: 116).

Claim 21; Bazinet et al, figures 1-3, disclose a method for controlling an output voltage (Vout) of a DC/DC converter (10), wherein the DC/DC converter includes a main switching element and a synchronous switching element (12, 14), the method comprising: generating a pulse signal (62) for controlling the output voltage of the DC/DC converter based on the output

voltage (Vout); generating a first drive signal (38, 40) which has substantially the same pulse width as that of the pulse signal (figure 3: 116) and supplying the first drive signal to the main switching element (12, 14); and generating a second drive signal using the pulse signal and the first drive signal and supplying the second drive signal to the synchronous switching element such that the main switching element and the synchronous switching element are turned ON and OFF alternately at different timings.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 8-10, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bazinet et al (US 5,627,460) in view of Nishimaki (US 2004104714).

Claims 3, 8-10 and 16; Bazinet et al, figures 1-3, disclose the claimed subject matter in regards to claims 1, 7 and 14 supra, except for the drive signal generation circuit includes: a first delay circuit which generates the first drive signal by delaying the pulse signal; a second delay circuit connected to the first delay circuit, the second delay circuit generating a delayed signal by delaying the first drive signal; and a synthesis circuit connected to the second delay circuit, and the synthesis circuit generating the second drive signal by synthesizing the pulse signal with the delayed signal.

Nishimaki, figure 8, teach a drive signal generation circuit (32) includes: a first delay circuit (327) which generates a first drive signal (14) by delaying a pulse signal (11); a second delay circuit (326) connected to the first delay circuit (327), the second delay circuit generating a delayed signal by delaying the first drive signal (14); and a synthesis circuit (321) connected to the second delay circuit (327), and the synthesis circuit generating the second drive signal (13) by synthesizing the pulse signal (11) with the delayed signal (326).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Bazinet et al to have a drive signal generation circuit that includes: a first delay circuit which generates the first drive signal by delaying the pulse signal; a second delay circuit connected to the first delay circuit, the second delay circuit generating a delayed signal by delaying the first drive signal; and a synthesis circuit connected to the second delay circuit, and the synthesis circuit generating as suggested by Nishimaki in order to provide a drive signal generation circuit that reduces power consumption (paragraph [0084]).

Claim 20; Bazinet et al figure 1 discloses the pulse signal generation circuit includes: an error amplification circuit (54) which compares the output voltage (Vout) and a reference voltage (2.0v) to generate an error signal; and a comparison circuit (32) connected to the error amplification circuit, and the comparison circuit comparing the error signal and a triangular wave signal (Vramp) to generate a pulse signal having a pulse width proportional to the voltage of the error signal.

6. Claims 4, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bazinet et al (US 5,627,460) and Nishimaki (US 2004104714) in view of Bridge (US 6,396,250).

Bazinet et al, figures 1-3, and Nishimaki disclose the claimed subject matter in regards to claims 3, 10 and 16 supra, except for the first and second delay circuits each include a plurality of inverter circuits.

Bridge figure 13 teaches a delay circuit with a plurality of inverter circuits used to a delay a signal by a predetermined delay time set by the number of inverter circuits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit combination of Bazinet et al and Nishimaki to provide first and second delay circuits each including a plurality of inverter circuits as taught by Bridge in order to delay a signal by a predetermined delay time set by the number of inverter circuits in the first and second delay circuits.

7. Claims 5, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bazinet et al (US 5,627,460) and Nishimaki (US 2004104714) in view of Matsuda (US 4,862,364).

Bazinet et al, figures 1-3, and Nishimaki disclose the claimed subject matter in regards to claims 3, 10 and 16 supra, except for the first and second delay circuits each include an integrating circuit having a resistor and a capacitor.

Matsuda teaches a delay circuit (28) using a capacitor and resistor as an integrator circuit in order to delay a signal to a differential amplifier circuit where the delay is determined by the time constant of the integrator circuit (col. 3 lines 35-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit combination of Bazinet et al and Nishimaki to provide for the first and second delay circuits to each include an integrating circuit having a resistor and a capacitor in order to delay the signal according to the time constant of the resistor and capacitor combination.

8. Claims 6, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bazinet et al (US 5,627,460) and Nishimaki (US 2004104714) in view of Jain et al (US 6,577,517).

Bazinet et al, figures 1-3, and Nishimaki disclose the claimed subject matter in regards to claims 3, 10 and 16 supra, except for the synthesis circuit includes a NOR circuit.

Jain et al, figure 7, teaches using synthesizing circuitry in combination with delay circuitry that includes the use of NOR gates to synthesize the signals therein.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit combination of Bazinet et al and Nishimaki to provide a synthesis circuit that includes a NOR circuit in order to synthesize the signals according to the logic of a NOR gate as taught by Jain et al.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US RE38,487 Isham et al disclose generating a first drive signal such that the first drive signal has substantially the same pulse width as that of the pulse signal.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/23/05

Gary L. Laxton
Primary Examiner
Art Unit 2838